**REMARKS** 

Claims 1-3 and 7-22 are pending in the instant application. Claims 4-6 are

canceled herein. Claims 1, 7-12, 15, 17, 20 and 22 are amended herein. No new matter

has been added as a result of the amendments.

**Drawings** 

The drawings are objected to in the outstanding Office Action. The specification has been

amended herein in a manner so as to obviate the objection to the drawings (see attached

amendment). Consequently, the Applicants respectfully request the withdrawal of the drawing

objections made in the outstanding Office Action.

**Specification** 

The specification is objected to in the outstanding Office Action. The specification has

been amended herein in a manner so as to obviate the cited objections (see attached amendment).

Consequently, the Applicants respectfully request the withdrawal of the objections to the

specification made in the outstanding Office Action.

Claim Objections

The Examiner objected to the Claims as containing informalities. The Claims have been

amended herein so as to eliminate any informalities (see attached amendments to the Claims).

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Consequently, the Applicants respectfully request the withdrawal of the objections to the Claims.

## 112 Rejections

The claims have been amended herein to obviate the rejection of Claims 1-22 under 35 U.S.C. 112. Therefore, the Applicants respectfully request the withdrawal of the rejection of Claims 1-22 under 35 U.S.C. 112.

## 102 Rejection

Claims 1, 3 and 5 (now canceled) are rejected under 35 U.S.C. § 102(e) as being anticipated by Gauthier et al. (U.S. Patent No. 6,188,241). The Applicant has reviewed the cited reference and respectfully submits that the present invention as is recited in Claims is neither shown nor suggested by Gauthier et al.

The Examiner is respectfully directed to independent Claim 1 which sets forth an embodiment of the present invention including:

... a circuit comprising an analog circuit and a digital circuit wherein said analog circuit comprises an analog input and an analog output, and said digital circuit comprises a digital input and a digital output; a wirebond pad; a processor; and a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor.

Claim 3 depends from Claim 1 and recites further features of the Claimed invention.

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Gauthier et al. does not anticipate or render obvious a microcontroller that includes a switching circuit and a wirebond pad wherein "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by the switching circuit to the wirebond pad as is recited in Claim 1. It should be appreciated that Gauthier et al. only discloses a microcontroller having a block of logic that is configurable to perform a selected logic function and to produce output signals that are coupled to corresponding I/O pads. As such, Gauthier et al. is concerned with the coupling of logic signals (e.g., digital signals) that are generated from a configurable block of logic to an I/O pad. By contrast, Applicants' Claim 1 requires that a switching circuit selectively connect at least one analog and/or digital input and/or output from a microcontroller that includes both an analog circuit and a digital circuit to a wirebond pad. Thus, the embodiment of the Applicants' invention set forth in Claim 1 provides that at least a digital or analog input or output be coupled to a wirebond pad through a switching circuit. Indeed, nowhere in the Gauthier et al. reference is it taught or suggested that in a microcontroller that includes an analog and a digital circuit "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by a switching circuit to a wirebond pad as is recited in Claim 1. Consequently, Gauthier et al. does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 1.

Accordingly, Gauthier et al. does not anticipate or render obvious the present claimed invention as is set forth in Claim 3 dependent on Claim 1. The Applicants respectfully submit

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that these claims overcome the rejection under 35 U.S.C. 102(e) as being dependent on an allowable base claim.

Claims 1-22 (claims 4-6 are canceled) are rejected under 35 U.S.C. § 102(e) as being anticipated by Lesea (U.S. Patent No. 6,246,258). The Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as are set forth in Claims 1-22 (claims 4-6 are canceled) are neither anticipated nor rendered obvious by Lesea.

The Examiner is respectfully directed to independent Claim 1 which sets forth an embodiment of the present invention including:

... a circuit comprising an analog circuit and a digital circuit wherein said analog circuit comprises an analog input and an analog output, and said digital circuit comprises a digital input and a digital output; a wirebond pad; a processor; and a switching circuit that selectively connects at least one of said analog input, said analog output, said digital input and said digital output to the wirebond pad under control of the processor.

Claims 2-3 and 7-22 depend from Claim 1 and recite further limitations of the claimed invention.

Lesea does not anticipate or render obvious a microcontroller that includes a switching circuit and a wirebond pad wherein "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by the switching circuit to the wirebond pad as is recited in Claim 1. It should be appreciated that Lesea only discloses an CYPR-CD00199

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analog to digital converter that is provided on a field programmable array (FPGA). Moreover, Lesea teaches that this construction is realized without adding special analog circuitry. By contrast, the microcontroller of Applicants' Claim 1 is realized by employing both analog and digital circuitry. Moreover, Applicants' Claim 1 requires that a switching circuit selectively connect at least one analog and/or digital input and/or output in a microcontroller that includes both an analog circuit and a digital circuit to a wirebond pad. Thus, the embodiment of the Applicants' invention set forth in Claim 1 provides that at least a digital or analog input or output be coupled to a wirebond pad through a switching circuit. Nowhere in the Lesea reference is it taught or suggested that in a microcontroller that includes both an analog and a digital circuit "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by a switching circuit to a wirebond pad as is recited in Claim 1. Consequently, Lesea does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 1.

Accordingly, Lesea does not anticipate or render obvious the embodiments of the present claimed invention as recited in Claims 2-3 and 7-22 dependent on Claim 1. The Applicants' respectfully submit that these claims overcome the rejection under 35 U.S.C. 102(e) as being dependent on an allowable base claim.

## 103 Rejection

Claims 1, 2 and 4 (canceled) are rejected under 35 U.S.C. § 103(a) as being anticipated by Dabral et al. (U.S. Patent No. 6,192,431) in view of Wirebonding: Reinventing the Process for

CYPR-CD00199 Serial No.: 09/893,050 Examiner: Mason, D. 12 Group Art Unit: 2111 MCMs by H.K. Charles, Jr., et al. The Applicants have reviewed the cited reference and respectfully submit that the embodiments of the present invention as are recited in Claims 1 and 2 are neither anticipated nor rendered obvious by Lesea.

Dabral et al. does not anticipate or render obvious a microcontroller that includes a switching circuit and a wirebond pad wherein "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by the switching circuit to the wirebond pad as is recited in Claim 1. It should be appreciated that Dabral et al. only discloses a method and system for configuring the pinout of an integrated circuit. Dabral discloses that this is accomplished by communicating first and second signals of a parallel bus in first and second configurations respectively to pinout ports that control the pinout configuration of an integrated circuit. By contrast, Applicant's Claim 1 requires that a switching circuit selectively connect at least one analog and/or digital input and/or output from a microcontroller that includes both an analog circuit and a digital circuit to a wirebond pad. Thus, the embodiment of the invention set forth in Claim 1 provides that at least a digital or analog input or output be coupled to a wirebond pad through a switching circuit. Nowhere in the Dabral et al. reference is it taught or suggested that in a microcontroller that includes both an analog and a digital circuit "at least one of said analog input, said analog output, said digital input and said digital output" are selectively connected by a switching circuit to a wirebond pad as is recited in Claim 1. In fact, Dabral et al. does not disclose a microcontroller at all. Consequently, Dabral et al. does not anticipate or render obvious the embodiment of the Applicants' invention as set forth in Claim 1.

CYPR-CD00199 Examiner: Mason, D. Serial No.: 09/893,050 Group Art Unit: 2111 The Wirebonding: Reinventing the Process for MCMs reference does not overcome the

deficiencies of Dabral et al. noted above. The Wirebonding: Reinventing the Process for MCMs

reference was employed in the Office Action to teach a wirebond pad and does not address the

deficiencies of Dabral et al. outlined above. Consequently, Dabral et al. and the Wirebonding:

Reinventing the Process for MCMs reference, either alone or in combination does not anticipate

or render obvious the embodiment of the Applicants' invention as set forth in Claim 1.

Accordingly, the Applicant also respectfully submits that Dabral et al. and the

Wirebonding: Reinventing the Process for MCMs reference, either alone or in combination

does not anticipate or render obvious the embodiments of the present claimed invention as recited

in Claim 2 dependent on Claim 1. The Applicants respectfully submit that this claim overcomes

the rejection under 35 U.S.C. 103(a) as being dependent on an allowable base claim.

Conclusion

In light of the above-listed remarks, the Applicants respectfully request allowance of the

remaining Claims.

The Examiner is urged to contact the Applicants' undersigned representative if the

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Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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